Target Applications

- Deep Learning Accelerators
- Datacenter Networking
- Cryptocurrency ASICs

IP Deliverables

Documentation

- Databook
- Implementation Guideline
- Package and PCB Guideline

Hard IP Deliverables

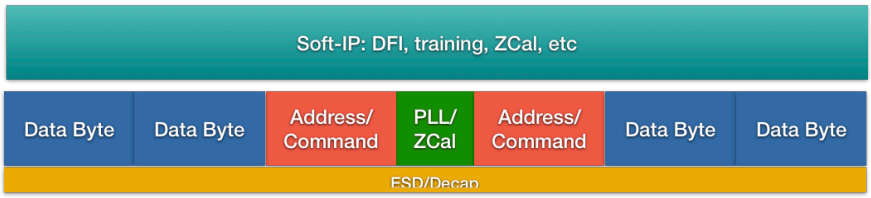
- Behavioral model (RTL)
- Layout abstract (LEF)
- Timing models (LIB/DB)
- Layout (GDSII)
- LVS netlist (CDL)
- Physical verification reports

Soft IP Deliverables

- RTL (Verilog)
- Synthesis & STA constraints

PHY construction

The GDDR6 PHY IP is delivered in both Soft-IP and Hard-IP components. The soft-IP component can be hardened upon request. For top/bottom die edge vs left/right die edge PHY instantiations, a different hard-IP view is available and would be required.



DFT Features

The GDDR6 PHY IP includes the following DFT features with bring-up observability and production testing in mind.

- Full-rate internal/external loopback
- PRBS generator/checker
- PHY independent testing
- I/O bypass mode for boundary scan
- Internal logic scan chain
- Analog and digital observation I/Os

For more information, please contact us at info@thesixsemi.com.