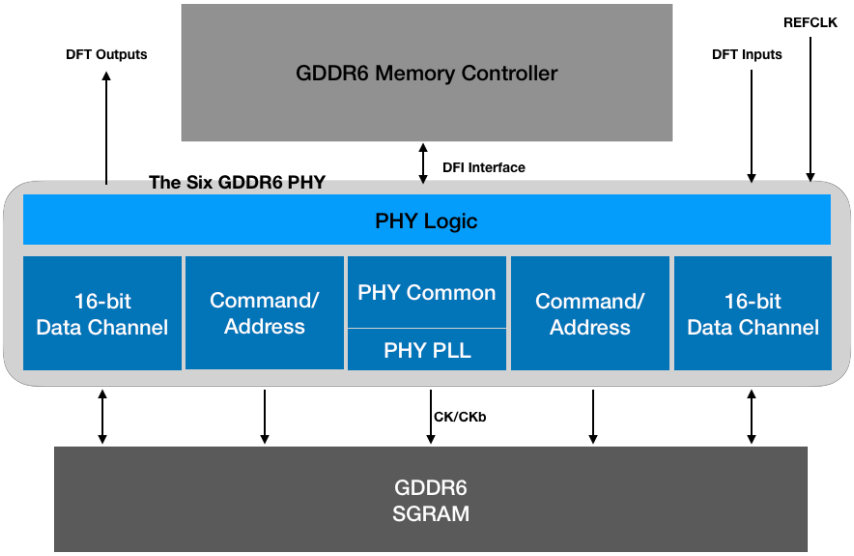
GDDR6 PHY IP

Key Feature

- 2x16-bit PHY instance
- Compliant to the following JEDEC standards:
  - JESD250 (GDDR6)
  - JESD232A (GDDR5X)
- PHY Independent mode training and calibration
- Continuous phase correction
- Channel equalization with transmit de-emphasis and receive CTLE/DFE
- Supports multiple frequency states with fast switching time
- Memory controller interface based on DFI
- Supports both POLY orientations
- ESD compliant to HBM2KV & CDM500V

Supported Data Rates

- GDDR6 - up to 16Gbps
- GDDR5X - up to 12Gbps



Overview

The Six Semiconductor Inc's GDDR6 PHY IP is designed to be fully compliant to multiple JEDEC standards for GDDR6 and GDDR5X support, with maximum data rate up to 16Gbps in GDDR6 mode. With full backward compatibility to the GDDR5X standard, the PHY provides flexible memory options for SOC platforms to optimize for specific price/performance target. The PHY is constructed as a 2x16-bit instance, complete with Command Address interface as well as shared PHY components.

The 2x16-bit GDDR6 PHY instance is complete with built-in hardware logic for CA, WCK2CK, Read and Write data eye training, as well as hardware for continuous phase tracking to compensate supply voltage and temperature drift.